# EAST Search History

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L2 | 1 | ((processor with (PLD FPGA) (programmable adh logic adj device)) and (program$4 same (simulat$3 verif$3 test$3 evaluat$3 anal$4)) and boolean and (register adj file)).clm. and ("716"/$.ccls. or "703"/$.ccls. or "714"/$.ccls.) | US-PGPUB | OR | ON | 2007/04/17 10:15 |